

SUE Design Manager

- **The Framework for All Design Capture, Simulation, Timing and Data Management**
- **Manage Circuits, Verilog, Documentation and Version Control**
- **Drive Third Party Simulation Tools**
- **Everything Needed to Manage Today's SOC Design Flow**

Manage Your Design with SUE

SUE is not just another schematic capture tool. SUE is a quantum leap in technology that gives the designer the ability to enter, visualize, and control large, complex chip designs. It is a complete design environment in which to capture all levels and types of design information.

Enter - Enter your designs using the simple graphical user interface. RTL Verilog, gate level, standard cells, or transistor level descriptions can all be entered into the same schematic. SUE can be used from architectural analysis down to transistor level schematics.

Visualize - The user can quickly and easily browse ALL levels of the design hierarchy. The designer can push from the top level RTL description all the way down to the transistor level with a click of the mouse. All Verilog, documentation, standard cell, and transistor level views can be observed from the same window.

Control - Through tight integration SUE can launch other point tools and review the results of those runs. SUE works interactively with most standard simulation and static timing analysis tools including Verilog, ADM, HSPICE, Pearl, PrimeTime, PathMill, IRSIM, and many more.

Simulation results are displayed right on your schematic! The interface is so seamless that in most cases the user doesn't even need to spend the time to learn how to run the other tool. From a single schematic, you can automatically generate SPICE, IRSIM and Verilog netlists. You can also attach the behavioral model to the schematic. Then,

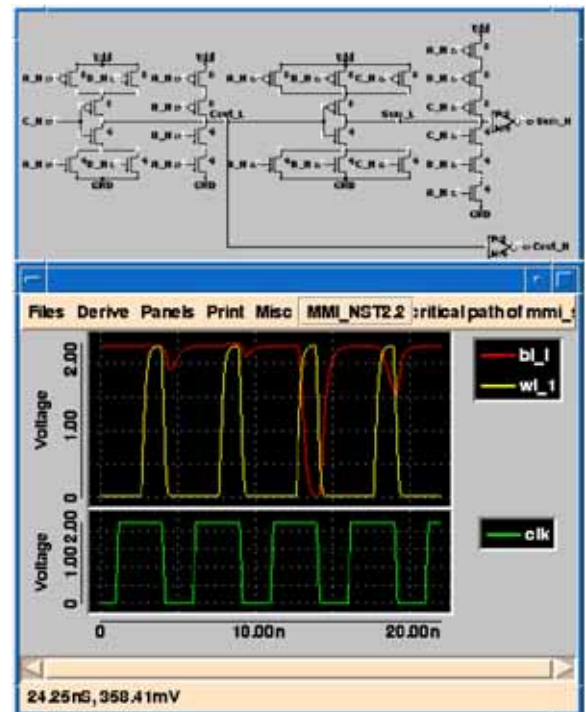


Figure 1-a.

View the Results of your simulation either directly on the schematic or in its waveform viewer.

when doing higher level Verilog simulations, you can choose whether to use the behavioral model or the schematic as input.

SUE allows easy extensions to its capabilities and it can be easily customized to fit into your existing environment.

Power for All Types of Designs

SUE is for the Architect who needs quick prototyping. Quick visibility through all layers of logic, and circuit design, give the Architect feedback to create high-performance architectures.

SUE is for ASIC or Semi-Custom designers who cannot currently achieve their IC performance goals in acceptable time-to-market.

SUE is for the Full-Custom design organization which wants complete control and visibility at all levels of design, and for whom performance is the name of the game.

SUE was conceived and written by IC designers who wanted a better environment to do their jobs. Everything the designer needs to enter designs, netlist them, and interact with analysis tools is included as standard equipment

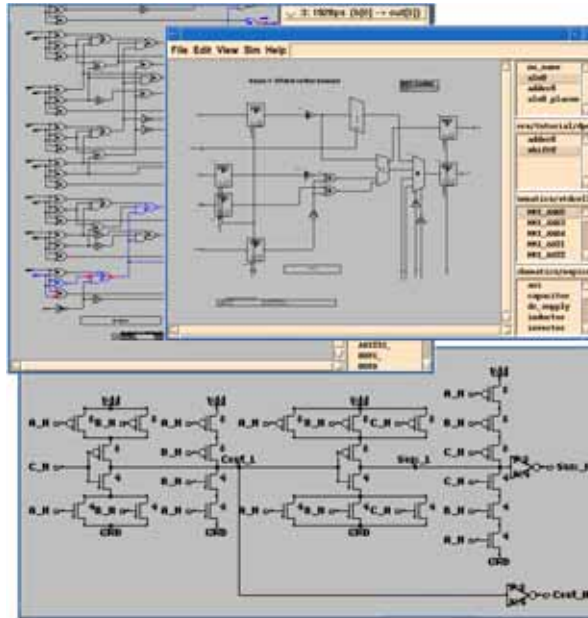


Figure 2-b. Use the power of SUE all the way from architecture analysis down to transistor level design.

SUE Features:

- Draw, view and edit schematics, icons, graphics and text.
- Automatically attach Verilog models and documentation to schematics.
- Automatic generation of Verilog from schematic symbols and vice-versa.
- Maintain multiple views (behavioral, RTL, structural) of schematics.
- Per-block choice of abstraction level at netlisting time.
- Interactive cross-probing during simulation on schematic or waveform tool.
- Includes Waveform Viewer and Reads/writes OVI compliant Verilog Files.
- ASCII database for transportability and ease of use with other programs, and revision control.
- Standard netlist and simulator interfaces.
- Complete Tcl/Tk programming interface and API.
- Complete on-line documentation.
- EDIF interface (optional).
- Available on LINUX platforms.

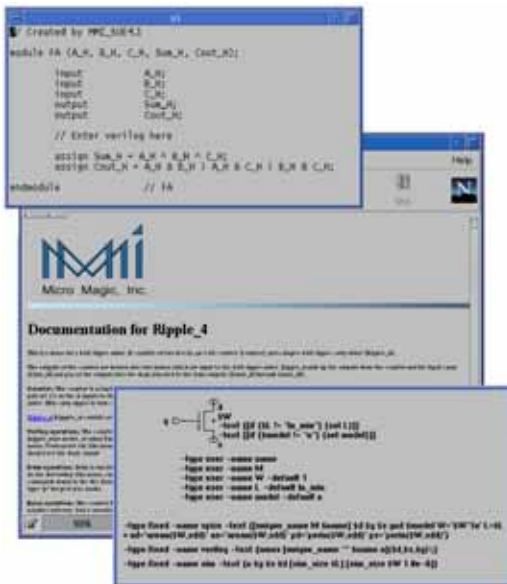


Figure 2-a. Manage documentation, Verilog, netlists and schematics with SUE

Micro Magic, Inc.
Sunnyvale, CA USA
Phone: 408.414.7647
www.micromagic.com