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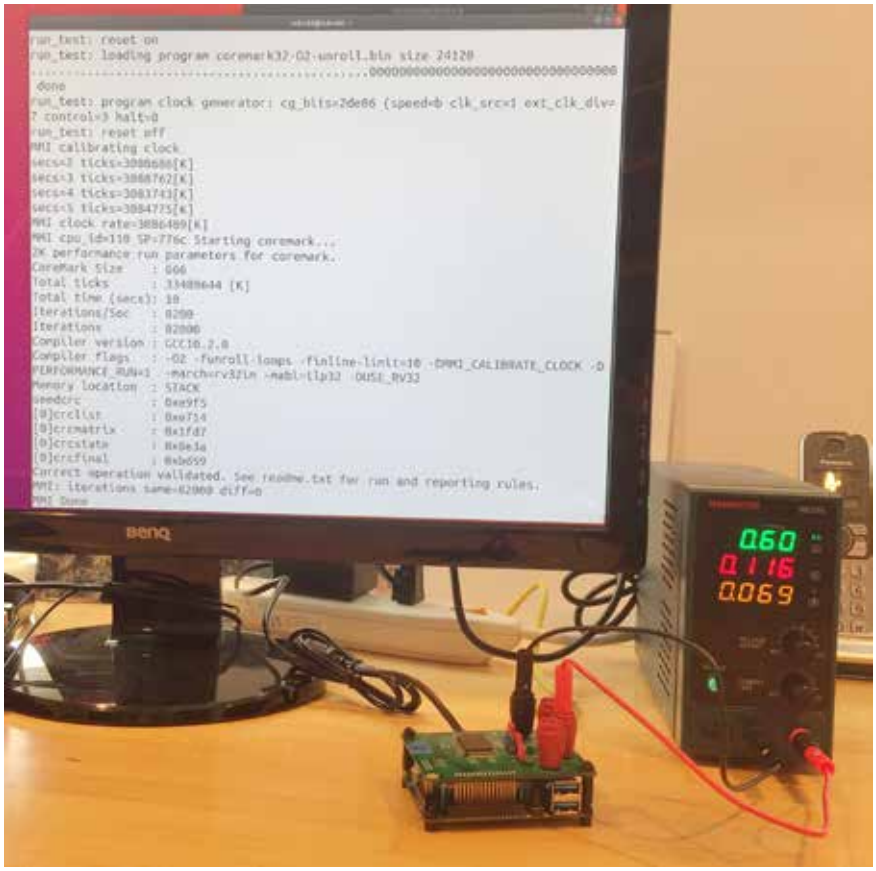
64-bit RISC-V core claims 10x better CoreMarks/Watt compared to other 3-5GHz CPUs

Dec 2, 2020 — by Eric Brown



Micro Magic RISC-V demo on Odroid board showing 110,000 CoreMarks/Watt

Micro Magic unveiled an up to 64-bit RISC-V core showing a groundbreaking 110,000 CoreMarks/Watt, with a 3GHz chip consuming less than 70mW. The company claims 10 times better CoreMarks/Watt compared to other processors in the 3-5GHz range.

Considering the spectacular promise and sudden demise of AI tech firm Magic AI, we should perhaps be wary of hyped up companies with Magic in their name. Yet, the astonishing claims about an incredibly efficient RISC-V core coming out of Sunnyvale, Calif. based EDA firm Micro Magic in recent weeks appear to be for real.

In late October, the company briefly announced a 64-bit RISC-V core achieving 5GHz and 13,000 CoreMarks at 1.1V. On Nov. 30, EETimes reported on a recent demo that appears to have matched the claims.

Today, Micro Magic announced another breakthrough, promising “the world’s highest performance/power 64-bit RISC-V core at 110,000 CoreMarks/Watt.” The Micro Magic RISC-V processor used in today’s 3GHz demo appears to be essentially the same as the similarly unnamed core in the EETimes demo running at 5GHz and 13,000 CoreMarks at 1.1V.

Today’s announcement shows 8,000 CoreMarks performance at 3GHz while consuming less than 70mW. This breaks down to 110,000 CoreMarks/Watt, which Micro Magic claims is 10x better than other CISC/RISC/MIPS processors in the 3GHz to 5GHz range.

Both benchmark demos were performed on silicon running on an unnamed Odroid SBC, which would suggest it is running Linux. The earlier demo showed 4.327GHz at 0.8V and 5.19GHz at 1.1V. The original October announcement claimed to demonstrate that a core “running at 0.8V nominal delivers 11,000 CoreMarks at 4.25GHz, consuming only 200mW.”

In the EETimes story, Micro Magic’s business liaison Andy Huang compared its benchmarks with the powerful new, 5nm fabricated Apple M1 system-on-chip for the Mac. While Apple claims the octa-core M1 delivers “the world’s best CPU performance per Watt,” the M1 breaks down to less than 100 CoreMarks per Watt, claims Huang, an industry notable who designed the Finesim simulator. Huang also compares its chip with the aging Cortex-A9 architecture, which he says is the fastest Arm processor in EEMBC benchmarks, performing at 1,112 CoreMarks per Watt.

Micro Magic is initially targeting battery-powered devices such as smartphones. “In today’s battery-operated devices, CoreMarks per Watt is much more important than CoreMarks per Megahertz,” Huang told EETimes. “For a typical 5W device, we can implement 25 cores. Who can do 25 cores in the mobile phone industry?”

In today’s press release, Micro Magic co-founder Lee Tavrow, along with fellow Sun alumnus Mark Santoro, also emphasized phones. “For applications like cell phones, it makes a big difference whether one can use their phone for a whole day, or several, on a single charge,” stated Tavrow. “Typically low power devices are also much lower performance, but with our IP, we allow our customer to have both the world’s fastest speed at 5Ghz and lowest power at 70mW and 3GHz in the same device.”

Micro Magic plans to use an IP licensing model for its RISC-V cores. We saw no details on when Micro Magic’s tech could start appearing in production silicon, and there is still no RISC-V page on the website.

Micro Magic is a leading EDA vendor specializing in 3D YSV layout tools, which it used to create its prototype silicon for the demos. The company was launched in 1995 and then sold to Juniper Networks for $260 million. In 2004, it was “reborn with the same name by the original founders,” says EETimes.

Tight coupling with fast memory

We found out about Micro Magic in this interesting, Nov. 30 ZDNet analysis of RISC-V developments,

which includes quotes from UC Berkeley professor David Patterson, who was a key developer of both RISC-V and RISC. “It’s kind of amazing,” Patterson told ZDNet of the initial Micro Magic demo. “I think IBM mainframes have a 5-gigahertz product that’s liquid-cooled and takes 100 watts.”

ZDNet notes that “The RISC-V chip has a score of 13,000, more than double the per-core performance score of the Arm-based Exynos. While the Intel Xeon is nominally higher per core, at 26,009, the Xeon part takes many more threads of execution, 120, to reach that performance.” While we know that CoreMark benchmarks are measured for just one core for each processor, we are not sure how the ZDNet determined that 120 thread number.

Huang hinted that one of the secrets to the core’s impressive power/performance ratio is a tight coupling with fast memory. “If memory is running at five gigahertz and logic is running at one gigahertz, who’s the bottleneck?” Huang told ZDNet, without disclosing further details. The story notes that in the early ‘90s Santoro and Tavrow patented an SRAM chip that at the time was the fastest on the market.

Huang explained to ZDNet that the simplicity of the RISC-V instruction set and openness of the architecture enabled Micro Magic to quickly develop the prototype using a standard silicon wafer with no special tweaking. This will also enable cost savings by small custom chip designers, which can pile onto a shuttle run where different chips from different vendors are fabricated on the same wafer.

There are further cost savings, of course, from not paying a licensing fee, as one would do with Arm. Huang added that RISC-V will help chip vendors and tech manufacturers meet expected regulations and market forces encouraging reduced power consumption.

The ZDNet story speculates on the potential for Nvidia to start developing RISC-V designs once it acquires Arm. Yet it is possible we have already passed the tipping point toward RISC-V. Unlike Arm, the RISC-V Consortium does not compel disclosure of use. In 2021 we are likely to see many new RISC-V chips spring to life fully formed out of secret R&D labs.

Recently, Alibaba’s RISC-V-focused T-Head subsidiary announced a collaboration with Allwinner to introduce a single-core, 1GHz XuanTie C906 (RV64GCV) RISC-V processor designed to run Debian Linux. For some recent updates on RISC-V activity, including SiFive’s recent FU740 SoC and HiFive Unmatched SBC, check out this Google Docs RISC-V slide deck from BeagleBoard.org’s Drew Fustini covering highlights of the Open Source Summit Japan 2020.

Further information

No timetable was mentioned for production of Micro Magic RISC-V based processors. More information may be found in the 110,000 CoreMarks/Watt announcement (PDF) and more should eventually appear on the Micro Magic website.