Micro Magic builds JAZiO test chip to prove new technology.
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Trimming a Third Off I/O Power Use

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One of the most exciting papers at the Embedded Processor Forum was not about a processor.

But few people in the audience were complaining as Jim Slager, chief evangelist with Jazio, presented details of a novel digital I/O scheme that he claimed could shave a third off chip I/O power consumption.

The technology could enable signal pin frequencies from 1GHz up to 4GHz while keeping signal slew rates at contemporary or lower levels, he said. Jazio is currently exploring licensing options with a number of major companies, and is considering requirements for standardising future DRAM architectures with Jedec.

Slager, a respected microprocessor designer who previously worked at Hitachi and Sun Microsystems, said the Jazio interface architecture could also have important implications for on-chip buses, although he restricted his presentation to the off-chip application of the interface.

Traditional bus signalling is based on a low voltage `0' and a high voltage `1' in near-to-square wave switching. But as clock frequencies have increased, more power is wasted in maintaining the classical signal form. The resulting wasteful effects include ground bounce, crosstalk, ringing and electromagnetic interference.

Reduced voltage swings, differential signalling on two wires and pseudo- differential signalling on a single wire have all been used to reduce sensing levels. But after doing all that, Slager observed, "all the information is transmitted during about a

third of the bit time; the rest of the time is just wasted".

Jazio's technology is a patented variation on low-voltage differential signalling. But the scheme is transition-sensitive whereas most conventional I/O schemes are level-sensitive. It only requires one pin per signal accompanied by two complementary free-running clock-like signals. These are the voltage timing reference VTR and its complement, VTR-bar. These signals ramp up and down in sequential clock periods.

Jazio's contribution is to invent a scheme that compares the data with VTR and VTR-bar and uses the outputs to check whether a transition has occurred or not. The steering logic that copes with the differential comparison, initialisation and registering a one or a zero requires 55 small-signal transistors.

Slager said that some people might complain at this overhead. But on multi-million transistor chips, an interface that occupies an area considerably smaller than a bond pad in contemporary process technologies is a small price to pay for the improved data rates it brings.

Slager asserted that the technique minimises slew rates, which can cause signal integrity problems and, because it so deeply and completely embedded in the physical layer, is applicable to any higher order communications protocol such as RapidI/O, double data rate RAM or Rambus DRAM.

Jazio recommends a sensing differential of about 500mV, which compares with 800mV or more for pseudo-differential signalling, and that a VTR and VTR-bar is included for every 18 data lines.

"If you want to go wider, that's fine, but we suggest replicating VTR and VTR-bar."

In his talk, Slager emphasised that most of the information to enable engineers to design with the Jazio interface would be put in the public domain but that Jazio demanded a licence agreement before chips were shipped.

When Slager was later asked how Jazio would police its patented technology, he said: "I don't think anyone would want to rip us off. Certainly, to use the technology and risk being prosecuted later would be very dangerous."

In the DRAM application Jazio has suggested a lifetime licence fee of $200,000 and a 0.3% royalty fee per DRAM sold, although the Jazio interface could also be applied to any digital logic chip.

Slager said that Micro Magic, a design services company that specialises in advanced design using internally developed EDA tools, is building a test chip to prove the Jazio technology. The company is using a 0.18 micro m process technology and expects to get Jazio pins toggling at 2GHz. Silicon is expected next month and samples should be available to potential licensees in the fourth quarter of 2000.

Slager said a move to 0.13 micro m should double the performance of the Jazio interface.

Vojin Oklobdzija, a professor at the department of electrical and computer engineering of University of California, with experience in I/O circuit design, said: "Standard ECL on bipolar uses a 800mV signal swing on-chip. Using 500mV off-chip is very advanced and the power savings are obvious. It's very good."

Jazio can be used for on-chip buses, Slager said, adding: "It can do that, if you think of highly integrated SoC designs with on-chip memory and very wide buses there are great opportunities, but first I've got to persuade people it's a good idea going off-chip."
