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1GHz RISC-V processor consumes 10mW

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A RISC-V processor core has been built, including level-one caches, that consumes just 10mW when operated in the voltage-threshold region at 350mV.

The core was developed by Micro Magic Inc. (Sunnyvale, Calif.), a long-standing processor design services firm and EDA tools developer. The company had already claimed that its design was the fastest 64-bit RISC-V processor (see EDA company claims world's fastest 64bit RISC-V core and RISC-V core out-clocks Apple, SiFive;

available as IP).

But in an interview with eeNews Europe Mark Santoro, CEO of Micro Magic, said the processor core had also been designed so that it can operate down to at least 350mV, near the threshold voltage of the manufacturing process. (see CEO interview: Silicon Valley is still the place where the magic happens). This allows a sacrifice in performance to achieve considerable power savings.

At 1.1V the RISC-V core operates at a clock frequency of 5.1GHz and consumes about 500mW. At 350mV the core can still be operated at a clock frequency of 1GHz and consumes just 10mW.

Micro Magic has chosen the CoreMarks benchmark from Embedded Microprocessor Benchmark Consortium (EEMBC) as a measure of performance. At 5.1GHz the processor achieves 13,333 CoreMarks and at 1GHz it achieves 2,500 CoreMarks.This gives CoreMarks per watt figures of merit of 26.6k CoreMarks/W at 5.1GHz and 250k CoreMarks/W at 1GHz. This means by reducing the voltage to a third and the clock frequency by a factor of five a power efficiency increase of more than 9 can achieved.

Micro Magic has made these measurements on real silicon manufactured using a multiproject wafer run. And no “binning” of chips was used in the benchmarking so the same chip can achieve both 5.1GHz (500mW) at 1.1V and 1GHz (10mW) at 350mV. This opens up the prospect of dynamic performance-power scaling.

What foundry? what process?

However, the company has declined to say what manufacturing process or foundry manufacturer has been used. The company has said the design uses a FinFET process and that it examined physical design kits (PDKs) from three leading foundries seeking the broadest compatability before selecting one for manufacturing.

The process is likely to be somewhere between 20nm and 10nm and from one of Globalfoundries, Samsung, SMIC and TSMC. Intel also manufactures using FinFET processes but is thought to have abandoned foundry business.

China’s SMIC entered mass production at 14nm in 4Q19 and the company specifically advertises the ability to support ultra-low working voltages and to operate cores with three different threshold voltages.

Santoro also points out that Micro Magic’s design bridges both the high performance computing demands of the datacenter and the low power consumption needs of the smartphone. These are the primary application fields for chip companies using leading-

edge 7nm and 5nm manufacturing processes. However, the open-source RISC-V architecture has yet to make significant in-roads in either application sector.

The chip demonstrates what the design house and its tools can achieve. It is thought to be a “calling card” design to help the company transition into intellectual property core licensing; the business model pioneered by ARM. However, in the interview Santoro said that decision is pending other developments.

Micro Magic was co-founded by Santoro and Lee Tavrow in 1995. Santoro had gained experience previously working at Weitek, Apple Computer and Sun Microsystems and Tavrow at Digital Equipment Corp. and Sun Microsystems. The team had experience in designing fast-access SRAMs and developed specialized design tools for timing-driven layout and datapath optimization. This lead to Micro Magic being acquired in December 2000 by Juniper Networks Inc. for $260 million. The founders of Micro Magic restarted the company in 2004 and have been working in EDA tool licensing and design services since then.